CLAIM AMENDMENTS

1. (currently amended) An on-chip multiple tap transformer balun comprises:

first winding operably coupled for a single-ended signal; and

a ~~plurality of~~ second windings operably coupled for at least one of a first differential signal and a second differential signal, wherein a first portion of the second winding~~plurality of windings~~ is symmetrical with a second~~fourth portion~~~~winding~~ of the second winding~~plurality of winding~~, and a ~~second winding~~ third portion of the second winding~~plurality of windings~~ is symmetrical with a ~~third winding~~ fourth portion of the second winding, and when the first differential signal is coupled to the second winding, the first differential signal is coupled across the first portion and the second portion of the second winding, and when the second differential signal is coupled to the second winding, the second differential signal is coupled across the third portion and the fourth portion of the second winding;~~plurality of windings~~

wherein the second winding is electrically isolated from the first winding and electromagnetically coupled to the first winding.

2. (currently amended) The on-chip multiple tap transformer balun of claim 1, wherein the second winding~~plurality of windings~~ comprises a substantially octagon interwound shape with a plurality of taps for coupling to the first and second differential signals.

3. (currently amended) The on-chip multiple tap transformer balun of claim 1 wherein the first winding is on at least one layer of an integrated circuit, the on-chip multiple tap transformer balun further comprises:

a shunt winding on a different layer of the integrated circuit from the at least one layer, wherein the shunt winding is coupled in parallel with the first winding.

4. (currently amended) The on-chip multiple tap transformer balun of claim 1, wherein the ~~plurality of windings~~ second winding further comprises:

fifth and sixths portions of the second winding~~windings~~ operably coupled for a third differential signal, wherein the fifth portion of the second winding~~winding~~ is symmetrical with the sixth portion of the second winding~~winding~~ and wherein the third differential signal is coupled across the fifth portion and the sixth portion of the second winding.

5. (currently amended) The on-chip multiple tap transformer balun of claim 1 wherein the second winding is on at least one layer of an integrated circuit, the on-chip multiple tap transformer balun further comprises:

a ~~plurality of~~ shunt windings on a different layer of the integrated circuit from the at least one layer, wherein the ~~plurality of~~ shunt windings is connected in parallel to with the second winding~~plurality of windings~~.

6. (currently amended) The on-chip multiple tap transformer balun of claim 1 comprises:

the first winding being on a first layer of an integrated circuit;

the second winding~~plurality of windings~~ being on a second layer of the integrated circuit, wherein the second layer is a metalization layer of the integrated circuit having lowest resistivity.

7. (original) The on-chip multiple tap transformer balun of claim 1, wherein the first winding further comprises multiple turns.

8. (cancelled)

9. (currently amended) The on-chip multiple tap transformer balun of claim 1, wherein the ~~plurality of windings~~ second winding further comprises:

a rectangular octagonal shape having a first dimension lengthened with respect to a square octagonal reference shape and having a second dimension shortened with respect to the square octagonal reference shape, wherein area of the rectangular octagonal shape is similar to area of the square octagonal reference shape.

10. (original) The on-chip multiple tap transformer balun of claim 1 further comprises:

an integrated circuit size based on a balancing of inductance values of the on-chip multiple tap transformer balun, turns ratio of the on-chip multiple tap transformer balun, quality factor of the on-chip multiple tap transformer balun, and capacitance of the on-chip multiple tap transformer balun.

11. (new) An on-chip multiple tap transformer balun comprises:

first winding on at least one layer of an integrated circuit, operably coupled for a single-ended signal;

a second winding operably coupled for at least one of a first differential signal and a second differential signal, wherein a first portion of the second winding is symmetrical with a second portion of the second winding, and a third portion of the second winding is symmetrical with a fourth portion of the second winding, and when the first differential signal is coupled to the second winding, the first differential signal is coupled across the first portion and the second portion of the second winding, and when the second differential signal is coupled to the second winding, the second differential signal is coupled across the third portion and the fourth portion of the second winding; and

a shunt winding on a different layer of the integrated circuit from the at least one layer, wherein the shunt winding is coupled in parallel with the first winding.

12. (new) The on-chip multiple tap transformer balun of claim 11, wherein the second winding comprises a substantially octagon interwound shape with a plurality of taps for coupling to the first and second differential signals.

13. (new) The on-chip multiple tap transformer balun of claim 11, wherein the second winding further comprises:

fifth and sixth portions of the second winding operably coupled for a third differential signal, wherein the fifth portion of the second winding is symmetrical with the sixth portion of the second winding and wherein the third differential signal is coupled across the fifth portion and the sixth portion of the second winding.

14. (new) The on-chip multiple tap transformer balun of claim 11 comprises:

the first winding being on a first layer of an integrated circuit;

the second winding being on a second layer of the integrated circuit, wherein the second layer is a metalization layer of the integrated circuit having lowest resistivity.

15. (new) The on-chip multiple tap transformer balun of claim 1, wherein the second winding further comprises:

a rectangular octagonal shape having a first dimension lengthened with respect to a square octagonal reference shape and having a second dimension shortened with respect to the square octagonal reference shape, wherein area of the rectangular octagonal shape is similar to area of the square octagonal reference shape.

16. (new) An on-chip multiple tap transformer balun comprises:

first winding operably coupled for a single-ended signal;

a second winding on at least one layer of an integrated circuit, operably coupled for at least one of a first differential signal and a second differential signal, wherein a first portion of the second winding is symmetrical with a second portion of the second winding, and a third portion of the second winding is symmetrical with a fourth portion of the second winding, and when the first differential signal is coupled to the second winding, the first differential signal is coupled across the first portion and the second portion of the second winding, and when the second differential signal is coupled to the second winding, the second differential signal is coupled across the third portion and the fourth portion of the second winding; and

a shunt winding on a different layer of the integrated circuit from the at least one layer, wherein the shunt winding is coupled in parallel with the second winding.

17. (new) The on-chip multiple tap transformer balun of claim 16, wherein the second winding comprises a substantially octagon interwound shape with a plurality of taps for coupling to the first and second differential signals.

18. (new) The on-chip multiple tap transformer balun of claim 16, wherein the second winding further comprises:

fifth and sixth portions of the second winding operably coupled for a third differential signal, wherein the fifth portion of the second winding is symmetrical with the sixth portion of the second winding and wherein the third differential signal is coupled across the fifth portion and the sixth portion of the second winding.

19. (new) The on-chip multiple tap transformer balun of claim 16 comprises:

the first winding being on a first layer of an integrated circuit;

the second winding being on a second layer of the integrated circuit, wherein the second layer is a metalization layer of the integrated circuit having lowest resistivity.

20. (new) The on-chip multiple tap transformer balun of claim 16, wherein the second winding further comprises:

a rectangular octagonal shape having a first dimension lengthened with respect to a square octagonal reference shape and having a second dimension shortened with respect to the square octagonal reference shape, wherein area of the rectangular octagonal shape is similar to area of the square octagonal reference shape.